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Transmission Line Pulse Testing of the ESD Protection Structures of ICs.- A Failure Analysts Perspective.

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Abstract

The IC industry continues to find ways to improve the ability to correlate the electrical failure signature of devices with the physical failure location using different techniques. The purpose of this work is to show that improved transmission line pulse (TLP) testing technique of ESD (ElectroStatic Discharge) protection structures can provide accurate identification of leakage current to better identify where ESD stress testing should stop and failure analysis should begin. Besides the traditional current and voltage measurements at the Device Under Test (DUT), this new TLP testing technique includes the ability to correct for the measurement system losses for improved accuracy. The pulse width of the TLP is chosen to provide the same current amplitude damage level (electrical) as is found in the Human Body Model (HBM) ESD stress testing. This allows a one to one correlation between the two methods and hence the means to correlate the electrical damage of the device and the physical location of the failure site. An SCR (Silicon Controlled Rectifier) device is used as an example.

Introduction

The use of failure analysis to confirm the physical location of a failure site in a device damaged by ESD stress testing is well established [1]. Fifteen years ago the Transmission Line Pulse (TLP) testing technique was introduced by Maloney and Khurana [2, 3] as a new electrical analysis tool. The tool employed a rectangular pulse with energy similar to that utilized in HBM testing to provide an equivalent energy threat to the ESD protection structures of ICs. TLP is a very short pulse measurement system which has evolved into a very useful tool to provide both electrical operating analysis, and electrical damage signatures (EDS). By using a flat top pulse, both the current through the device under test (DUT) and the voltage across the DUT can be accurately measured to provide its Current-Voltage (I-V) characteristics. During this same time, we saw the sporadic use of failure analysis to confirm the physical location of the failure sites due to TLP testing [4-7]. HBM testers were built to simulate real life HBM in qualifying ICs to specified immunity levels [8, 9]. Initially, HBM stress testing was used for analysis of ESD designs to determine if they met the desired level of immunity. As TLP became available to more IC manufacturers, it quickly replaced HBM for design work.

Home made TLP test equipment systems has been used for many years [2, 3 10] but undefined measurement errors required considerable expertise to interpret the data from each different system. However, it was the only method that could provide the dynamic electrical characteristics of each ESD protection design at high pulse currents. As ESD designers provided data showing fairly good relationships between TLP and HBM testing, it became more widely used and its test data became more accepted as an effective design analysis tool. With the use of Failure Analysis tools, they were able to show that TLP can correlate to HBM peak current amplitude failures and also to the failure sites located. This correlation has been remarkable because the HBM ESD event uses a double exponential and the TLP ESD pulse uses a square or rectangular pulse. HBM pulses with an exponential decay (1/e) time of 150 nsec should theoretically require a rectangular pulse of 75 nsec to provide an equivalent energy at the same peak currents [10]. Traditional HBM ESD testing for qualification [8] requires the use of a discharge circuit of a 1500 ohm resistor and 100 pF capacitor connected in series. The resulting stress pulse is a double decaying exponential waveform with most standards specifying a rise time of 2-10 nsec.

ESD designers have been using TLP systems with rectangular pulse widths of 75-200 nsec with unspecified rise times that have probably ranged

between 1 nsec and 40 nsec. When attempting to compare failure from TLP pulses to HBM pulses, the rise times of both systems must be considered in addition to the pulse widths. The rise time of either threat pulse however, can cause significant differences in device failures because of dV/dt effects in the layout and arrangement of components in the ESD protection circuit.

Most designers however, fail to provide evidence of physical failures for both types of testing in the same paper [11-17]. Those who do, have not addressed the critically relevant issue of risetime of both the TLP and HBM pulse [18-20]. This is probably because of the difficulty of controlling this parameter. Those who do consider the rise time do not provide any physical (FA) pictures [21-26]. Correlation between the rectangular TLP pulse and the double exponential HBM test pulse can be remarkably close if the test pulse risetimes are comparable [27]. The ESDA standard risetime specification for the HBM test pulse has been 2 to 10 ns for many years, but most HBM testers built for testing 256 pins or more have a 9-10 ns risetime pulse [28].

HBM testers can only provide simple go/no-go test data, but the simplest TLP systems can provide Current-Voltage (I-V) data of ESD protection circuits and can be displayed on the tester or plotted on the computer screen with a software plotting program. This is a significant improvement for ESD design because it provides an analysis tool unavailable with HBM. Moreover, TLP also has the ability to measure and display the DC leakage current evolution of the device under test, that is, leakage measurement after each pulse instead of at the beginning of the stress test and at the end of the stress test. Adding a DC leakage current measurement of the DUT after each test pulse allows additional insight into minute changes of damage to the protection or core circuits, which is unavailable without this measurement. The DC leakage current data combined with the I-V data provides electrical indications of where damage begins, and how rapidly it can evolve from soft to hard failures. We define this I-V and leakage data on a device as the electrical damage signature (EDS).

TLP Basics

TLP is defined as the application of a narrow (75-200 nsec) rectangular pulse, usually generated by discharging a transmission line, to an ESD protection structure connected to the pins of an IC [23]. When the DUT voltage and current are measured it becomes a Pulse Curve Tracer [29] that has an energy content similar to that used in HBM ESD stress testing. With an ordinary curve tracer, the much higher amounts of energy associated with the longer pulse widths (usecs) dissipated in the ESD protection circuit, limits the current trace to a small fraction of what the same circuit is capable of with shorter ESD pulses. TLP Pulse stress testing to failure levels provides a peak current that compares to the peak HBM current that also fails the device under test.

When HBM is used for its primary purpose of qualification testing it stresses both the ESD protection circuit and protected core of the IC. When TLP is used in its primarily function as a design tool, it has the additional analysis advantage that allows testing each element used in protection structures to determine their individual pulse current capability and dynamic I-V characteristics. This provides the designer with knowledge on how each will perform in the final circuit assembly. Knowing the current path a stress pulse takes through an ESD protection structure and its dynamic impedance at I and V values allows the optimum design of each element. Each diode, transistor, resistor and metal interconnection can be individually TLP stress tested to provide a library of component size, layout, and optimum construction to be used in a complete ESD protection circuit. It can provide clear electrical failure analysis data on the voltage-current characteristics of each component. When the length of the test pulse is included, the energy capability of the elements is available.

A TLP pulse curve tracer (TLP-CTR) is an excellent electrical analysis tool because it uses rectangular pulses with a flat top [29]. This allows accurate measurements of both the voltage across the device and the current through the device by averaging the digitized data for some length of time near the end of the pulse. Testing the complete IC using the TLP pulse curve tracer provides an I-V characteristic curve which identifies the electrical behavior of the tested pin relative to a grounded pin

We made measurements using a constant impedance TLP system, which we define as TLP-50 (Figure 1). We define this because it uses a constant impedance of 50 ohms throughout the system up to the pads of the Device Under Test (DUT).

One of the advantages of maintaining a 50 ohm constant impedance for the pulse traveling through the system is that the pulse rise time and flat top of the TLP pulse is passed through constant impedance connections and is not degraded. Using the circuit arrangement of Figure 1, allows the DUT to be momentarily disconnected from the pulse source after each pulse with a coax switch so that DUT can be connected to a DC voltage source and pico ammeter. During this time a DC leakage measurement at the selected DC voltage (usually Vdd +/- 10%) is made after every test pulse with the DUT in situ. The

leakage current measurement is then plotted with the I-V plot, against the measured pulse current (that is, the current through the DUT). The constant impedance system allows both the DUT response and DUT leakage measurements to be made when testing either socketed devices or when TLP stress testing on wafers.

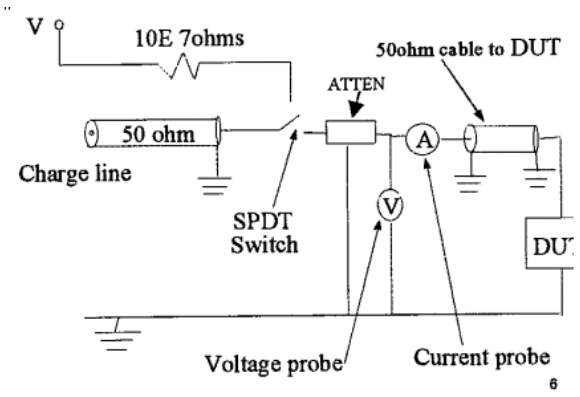

Figure 1 TLP-50: a constant impedance 50 ohm TLP system.

Some researchers have published data on the use of the traditional Curve Tracer (CTR) to stress test the ESD protect structures [30]. However, since the CTR uses extremely long pulses (μsec rise time and pulse width), it causes additional joule heating and EOS type failures. These longer pulse currents cause the ESD structures to fail at lower currents than that caused by the much shorter length ESD pulses. The CTR pulses are much longer (μsec) than HBM 150 nsec ESD pulses or the 100 nsec TLP pulses. TLP has typically used 100 ns long rectangular pulses to produces failures at the same peak currents as HBM. Damages seen from CTR failures are immediately visible after de-capsulation and occurs on the top surface of the device [31]. These are EOS failures compared to ESD failures which occur in the subsurface of the IC [32] and which require de-processing down to the silicon level to see the physical failures.

Calibration and Verification

Short and Zero ohms

At any point along the transmission line, there exists a source impedance of 50 ohms and a load impedance of 50 ohms. To be certain that measured TLP data is accurate, a TLP test systems must be calibrated and then verified that the pulse calibration factors are correct. TLP systems lend themselves to easy calibration by making a series of tests using a short (zero ohm) and an open (infinity ohms). Another low value resistor can be used that has a similar slope to the slope of the dynamic resistance of protection structures when in their high current conduction mode. A common value we use is 5 ohms.

Zero Ohm (short) Load Impedance

The figure 2 below shows that the transmission line is terminated with a load impedance of 0.00 ohms. Theoretically, the maximum current in the 0.00 ohms load is (500v/50 ohms) equal to 10 amps. This 10 amp maximum is achieved by the TLP-50 system. The voltage pulse is reflected back to the source with opposite polarity and the correct I-V curve is a vertical current line with "zero" voltage as shown in figure 3 . Hence the ideal TLP system shou ld not add any "unwanted" voltage to the measurements.

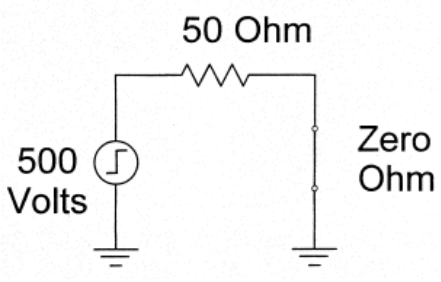

Figure 2 Basic calibration with short circuit (zero ohm).

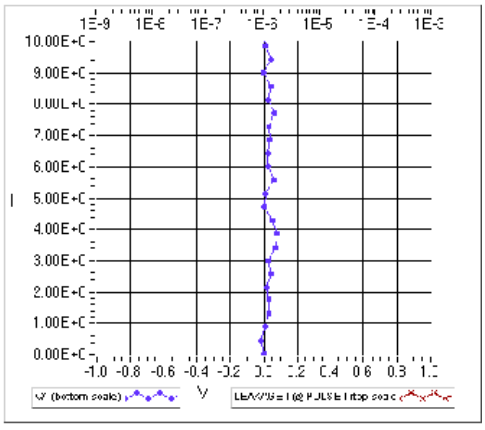

Figure 3 Typical short circuit calibration Plot.

Infinity Ohm (Open) Load Impedance

The figure 4 below shows a transmission line terminated with a load impedance of infinity ohms (open circuit). Theoretically (500 V/ ∞ Ω) there will be no current flowing in the circuit. Here the voltage pulse is reflected back to the source with the same polarity and the resulting I-V curve is a horizontal line shown in figure 5.

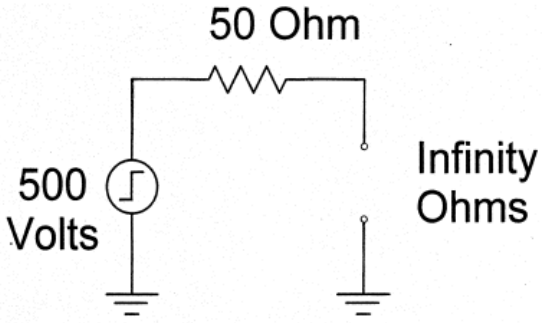

Figure 4 Calibration with open circuit.

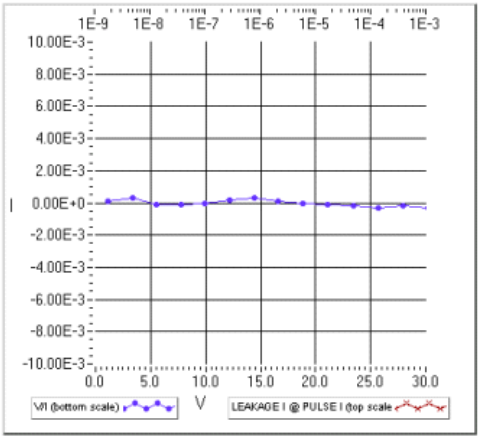

Figure 5 Typical open circuit calibration Plot.

5 Ohm Load Impedance

The figure 6 below shows a transmission line terminated with a load impedance of 5 ohms (device on impedance). Theoretically (500 V/ 55 Ω) there will be 9.0 amps in the calibration circuitry and the curve (diagonal line) is as shown in figure 7. Note that for a 50 ohm load impedance, the maximum current in the circuit is 5.0 amps, and a similar diagonal line is obtained if the transmission line is terminated with a 50 ohm impedance.

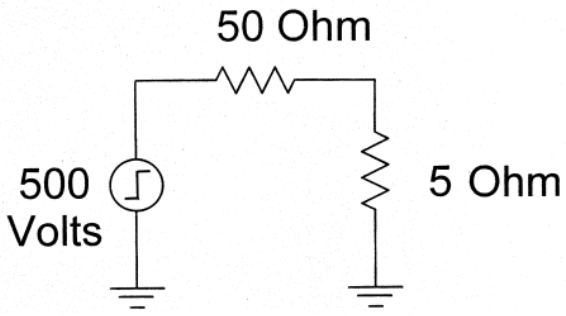

Figure 6 Calibration with 5 ohm load.

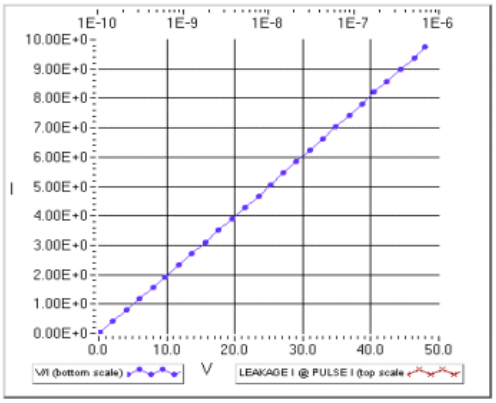

Figure 7 Typical 5 ohm calibration Plot.

Since the perfect short circuit (zero ohm) will have a perfectly vertical straight line with no voltage variations, the amount of the voltage variation is a measure of the short circuit measurement error [33]. This applies also to the open circuit measurement which results in the horizontal line. Further details are to be found in references [29] and [33].

The Gaussian Waveform

The broad tolerance of 2-10 nsec range in rise time as specified in the HBM standard adds to the correlation problems. The risetime variation and added ringing of the HBM tester is avoided in the TLP-50 by using controlled 0.2 nS, 2.0 nS, and 10.0 nS Gaussian shape risetime pulses. Controlled Gaussian rise time test pulses with no overshoot or ringing as shown in Figure 8. These Gaussian waveforms are used because they transition gradually as do most "real-life" HBM threat pulses. The Gaussian waveforms are obtained with special filters that can produce the initial rise in a gradually increasing and controlled manner. High voltage pulses in nature are usually produced this way, so being able to repeat the shape of the initial rise provides an inherent simulation of naturally occurring threats. Such risetime information could also provide data for the fundamentals of a TLP standard test method or standard practice.

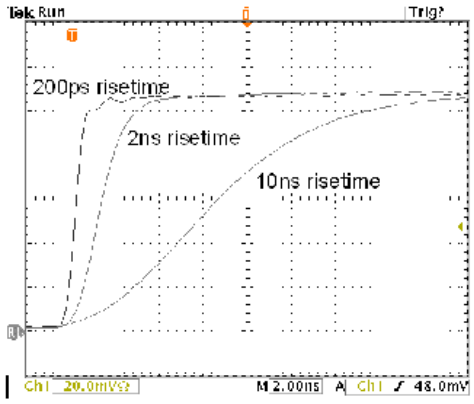

Figure 8 displays the 0.2 nsec, 2.0 nsec, and 10.0 nsec Gaussian rise times without any ripples.

The TLP Load Lines

The use of the load line concept to define the pulse current and voltage capabilities of any TLP system is shown below in figure 9. The first load line represents the 50 ohm load line at the maximum test pulse amplitude of 500 volts and the second is at half maximum amplitude. The figure 9 shows that the TLP-50 has a maximum pulse current of 10 Amps into a short circuit and a maximum pulse voltage of 500 Volts into an open circuit or infinity ohms. The different slopes of constant resistance plotted with the TLP system are all shown starting at the origin, and are labelled characteristic lines. The open (infinity ohm) circuit horizontal line and the short (zero ohm) circuit vertical line are obvious in figure 9. Note however that the "playing field" area for designers is much smaller than the 500 volts indicated in figure 9. We can attribute this to the fact that designers deal with single protection structures and not packaged ICs where other circuit interactions come into play.

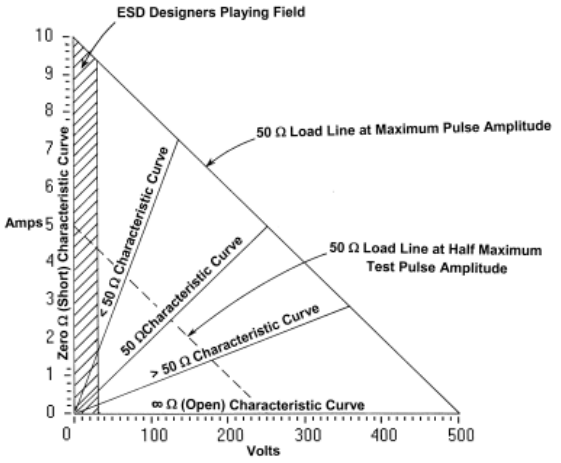

Figure 9 The Load line of the TLP 50 at the maximum test pulse amplitude and at half of the

maximum pulse amplitude.

The Device Negative Resistance

The 50 ohm operating load line for the TLP-50 identifies how the system operates in the negative resistance portion of a device with snap-back. When the test pulse amplitude is in the negative resistance region of a DUT, it can only plot out the actual I-V data if the absolute value of the negative resistance portion of the DUT is lower than the source impedance of the TLP. In the case shown in Figure 10, the slope of the TLP system load line is lower [50 ohms] than that of the DUT negative resistance line [125 ohms]. The TLP will be able to accurately identify the peak voltage immediately before snap-back (trigger voltage, Vt1); but when it increases above the snap-back point (at the far right in figure 10), it will immediately snap to a current and voltage on the positive resistance portion above the holding current. [33]. The details are covered in reference [33].

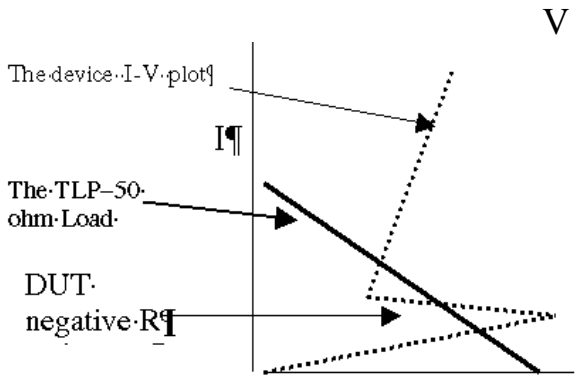

Figure 10 The TLP 50 Load line crossing the I-V plot of a typical DUT.

Stress Testing ESD Structures

It is important to distinguish between single element ESD structure stress testing and full IC (chip) stress testing. Based on the data in the literature, most TLP stress testing is used for single element stress testing during design and HBM stress testing is used for IC qualification testing [8]. However HBM and TLP correlation is necessary to extrapolate the TLP ESD results to full chip HBM stress testing. TLP stress testing was probably never intended as a direct replacement of HBM; however its simplicity and accuracy is leading toward its use as a calibrated and more universal and quantifiable reference. The HBM stress testing is relatively good because it represents a go/no-go stress test (pass or fail), but it provides very limited data. On the other hand, TLP stress testing of single structure elements gives the detailed data that is needed by the designer. Whereas TLP can be regarded as an engineering tool, the HBM stress test is a qualification tool which provides levels of threshold

failures, that is, classes like 1, 2, 3 etc which are related to the increase in voltage failure levels.

Stress testing single structures (diodes, resistors, capacitors, transistors, metal stripes etc) will provide direct insight into the single protection structures. This is done either on a wafer or packaged as test chips or test devices before qualification. At qualification , the fully packaged IC (ESD structure + core) is stressed tested. The electrical I-V characteristics may be somewhat different but the physical failure location is the same – inside the protect structure.

The most common way to stress test the single protection structures is to use wafers level stress testing. For the diode, there is junction failure which is localized for the reverse breakdown and spread nicely along entire width of the structure for the forward breakdown. Three types of failures occur for a transistor: the failure at the gate-drain junction (avalanching junction); the second failure type is the failure at silicide block edge in the drain [36]; the third is the gate oxide failure which has been reported by H Gieser [37].

What Is Stress Tested

In general, for the MOS devices, the drain (collector) is stress tested while the gate , the source (emitter) and the substrate are tied to ground. This is an example of a single element structure.

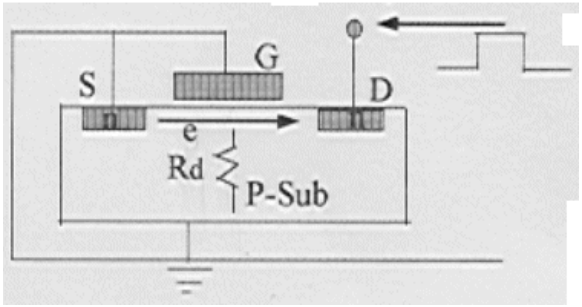

Figure 11 Schematic showing the protection structure is stress tested.

The wafer level can be used to test a single element structure or a combination of several structures. Figure 12 shows the path of the current through the protection structure and the resulting I-V characteristic curve is on the right (pin 1 to Vss).

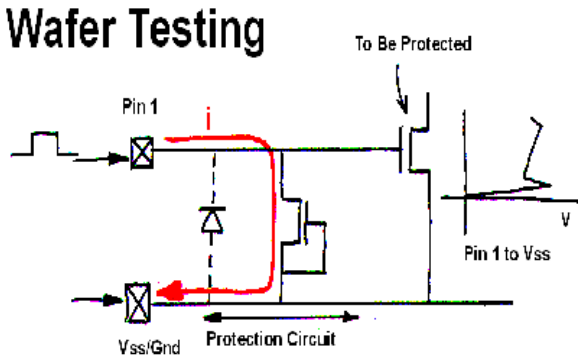

Figure 12 The protection structure on a wafer with the first protected core element.

The packaged test chip is a packaged single structure or several structures for design development testing. Each structure (resistor, diode or transistor etc) on the test chip has its own set of contact pads, bond wires to a lead frame and pins that can be contacted for testing. This figure 13 shows the resulting I-V curve for each structure.

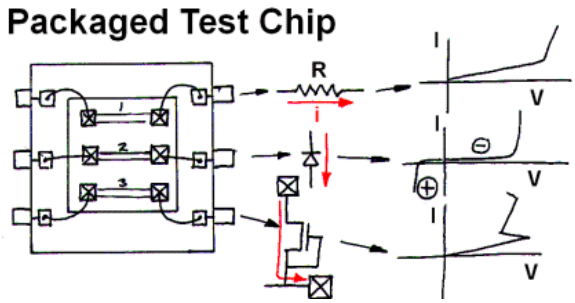

Figure 13 The layout of typical elements on a test chip for testing individual components.

The fully packaged IC is a combination of one or more of the single protection structures plus the core all connected by the usual metal stripes and interconnects of various widths. This figure 14 shows the different current paths and the interactions. In general, the I-V characteristic curve is the same with some variations due to interactions with the other elements on the IC.

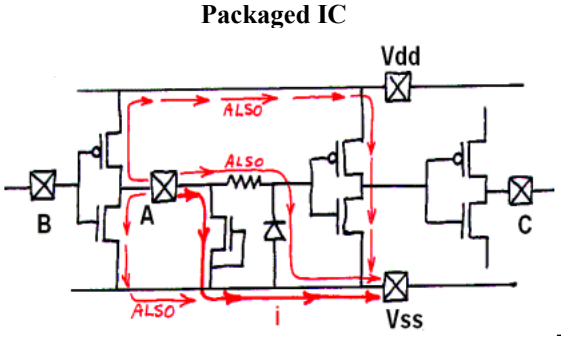

Figure 14 The layout of the fully packaged IC

(protection + core).

Basic I-V and Leakage Evolution Plots

The following three figures represent the characteristic responses from a typical nMOS device. There are two curves. In figure 15, the plot with the dots represent the I-V characteristic curve using the bottom x-axis (voltage) and the vertical y-axis (device current). The second plot with the crosses is a leakage evolution plot. After the collection of each I-V data point, a simple DC leakage measurement is done on the device under test. This DC leakage value (top x-axis) is obtained for a specified DC bias (e.g Vdd+10%) and is then plotted as a function of the stress parameter, the TLP pulse current (y-axis). In this figure, the structure shows no sign of a problem based on the I-V curve. However, the leakage evolution continues to change from pico amps to nano amps which is three orders of magnitude. Something has changed in the device and it is safe to say that the structure is damaged. Such electrical signatures are usually termed soft failures.

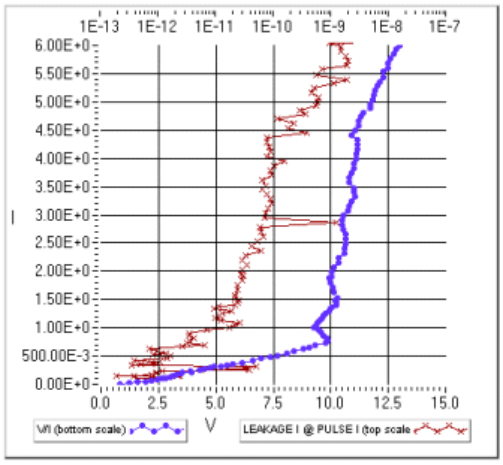

Figure 15 Soft Failure from TLP I-V plot.

In the figure 16, the I-V plot (dots) indicates an It2 point at 2.2 amps. The figure also shows that the leakage changes from 10E-10 amps to 10E-6 amps which is 4 orders of magnitude. This electrical data indicates a failure which appears to be catastrophic.

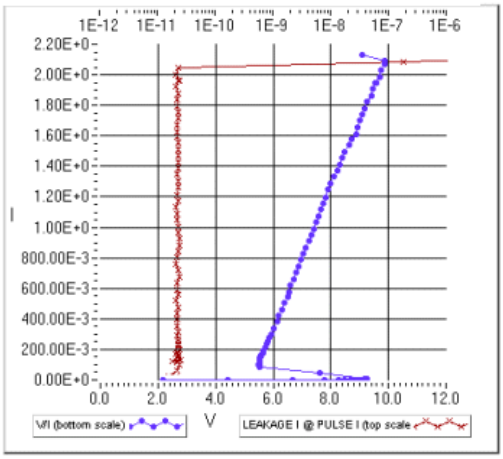

Figure 16 Hard Failure plot showing

For figure 17 below, a soft failure mechanism at 4.0 amps (vertical scale) appears before the hard failure at 8.6 amps. The leakage evolution allows the analyst to stop the stress at the soft failure point to perform physical failure analysis. This will allow identification of the physical location of the start (weakest point) to the failure if multiple failed locations are possible/expected.

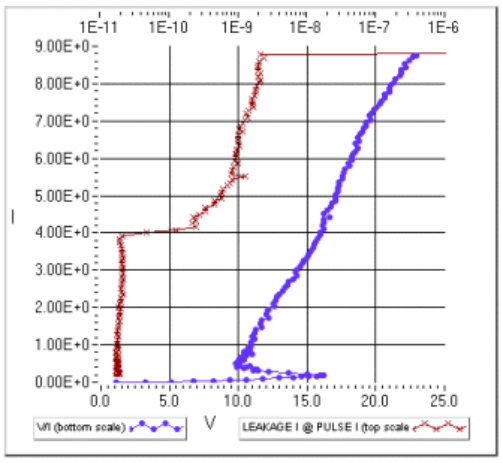

Figure 17 Soft failure followed by a hard Failure

Stress Testing the SCR Structure

We stressed several SCRs (silicon controlled rectifiers) type structures (figure 18). We made the measurements using a constant impedance TLP system, which we defined earlier as TLP-50 (figure 1). The basic SCR is a two terminal device made up of two transistors (G2 is pnp and G1 is npn), and the on-resistance typically ranges from 1-3 ohms. This is a low powered dissipating device so it is generally regarded as a good device for ESD protection. The designated anode pins (22 and 23), were each stress tested relative to the ground pin which is the Cathode in the structure.

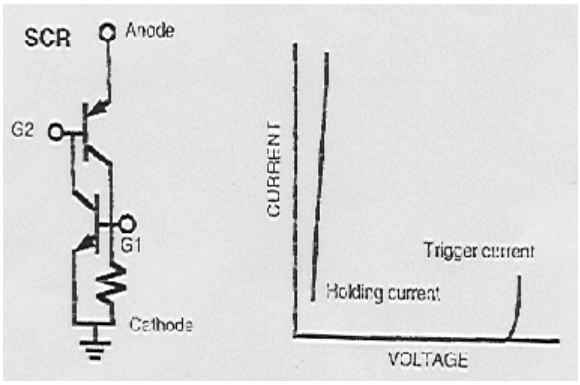

Figure 18 The schematic and I-V for a typical SCR structure.

The I-V characteristic of an SCR type structure (also called pnpn type structure or thyristor) is shown in figure 19 below. The I-V curve (dots) shows a trigger voltage (Vt1) of 6.4 volts, the typical snap-back region and a constant leakage evolution (vertical line-x's) of approximately 2.5 nanoamperes (2E10-5amps), the top horizontal scale. At approximately 3 amps (vertical y-axis scale), the structure appears to fail catastrophically with a leakage change of at least three orders of magnitude (10E-9 → 10E-6). The figure 19 I-V curve shows that this corresponded to the Vt2 of about 7.1 volts and a corresponding It2 of 3amps. For both the HBM and the TLP Step stressing, there was no leakage change until after catastrophic failure point at 3.0 amps. The snap-back or holding voltage, Vh (extrapolation of snap-back/resistance line) is approximately 1.60 volts and the on resistance is approximately 1.46 ohms.

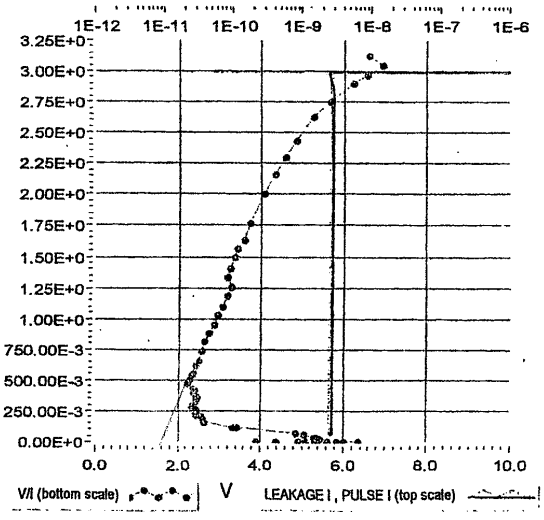

Figure 19 The I-V characteristic curve. and leakage evolution for the SCR.

Failure Analysis

These SCRs, which are single element pnpn transistor structures, were electrically tested using the Curve Tracer (CTR) and were found to exhibit the short-type electrical failures. Both anode designated pins (22 and 23) were tested to the designated ground pin- the cathode. After decapsulation and deprocessing, the physical failures could be seen as pits and deep"cuts" in the structure. The figure 20 shows the positive anode on the left side and the negative cathode anode on the right side of the figure.

For pin 23, the TLP low magnification 5KX SEM picture (figure 20) shows soft-failure sites (anode area) and the catastrophic or hard failure across the structure (anode to cathode).

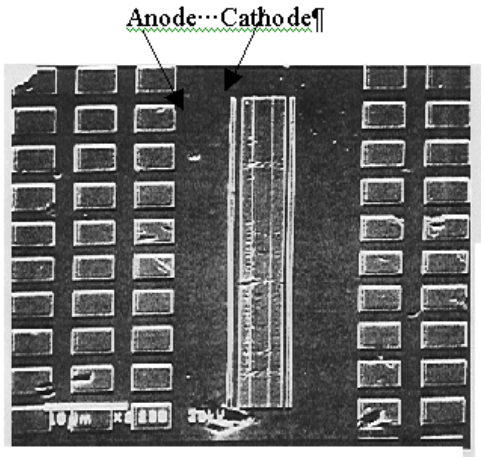

Figure 20 SEM photo of the TLP failure of the SCR protection structure for the anode pin 23.

The Figure 21 below shows the high magnification TLP failure from figure 20. The catastrophic failures across the structure from the anode to the cathode is quite evident. These 0.18um CMOS test structures failed at 3.6 KV for the HBM stress testing and 2.3 amps for TLP stress testing. The ratio (3.6/2.3) is 1.6 and is termed the correlation factor. The possible explanation for the multiple damage sites in the TLP pictures is that the high leakage started before the It2 point is reached, where the catastrophic failure frequently occurs.

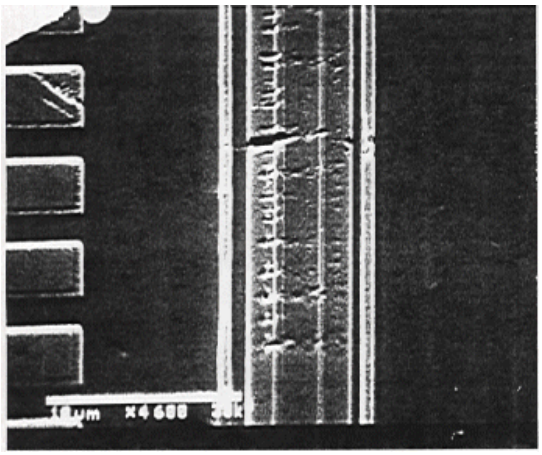

Figure 21 Higher magnification of the SEM photo of the TLP failure for pin 23 shown in figure 20.

For the same pin 23, the 14Kx magnification HBM picture below (figure 22) shows a much more severe and localized catastrophic failure but the failure location for this TLP failure is generally in the same anode area as the TLP failure site (figures 20 and 21).

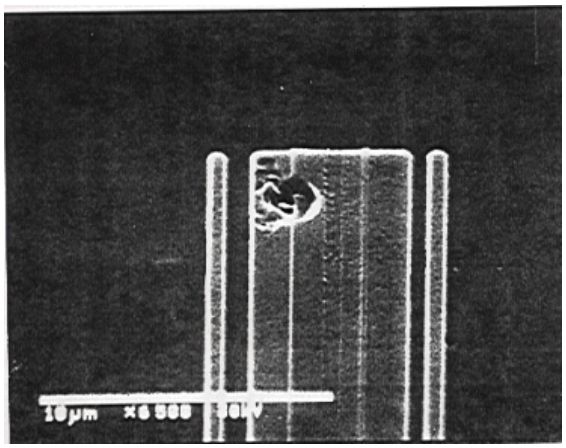

Figure 22 SEM photo of the HBM failure of the SCR protection structure for the same anode pin 23.

For pin 22, the low magnification HBM picture below (figure 23) also shows severe/catastrophic failure and the failure location is in the same anode area as the TLP and HBM failure sites for pin 23. The second (figure 24) and third pictures (figure 25) show the higher magnifications for pin 22. The pictures show "pits" and "cuts" not only in the anode area but across the structure from anode (left) to cathode (right). These 0.18µm CMOS test structures failed at 4.2 KV for the HBM stress testing and 2.75 amps for TLP stress testing. The ratio (4.2/2.75) provides a correlation factor of 1.5, which is similar to that (1.6) obtained for pin 23. We have therefore shown that both the TLP and HBM data exhibit failure location and failure type/signature correlation.

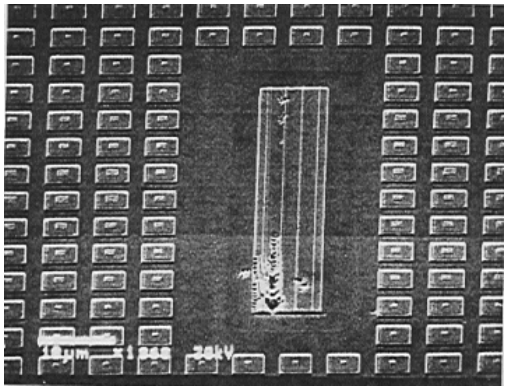

Figure 23 Low magnification SEM photo of the HBM failure of the SCR protection structure for the anode pin 22.

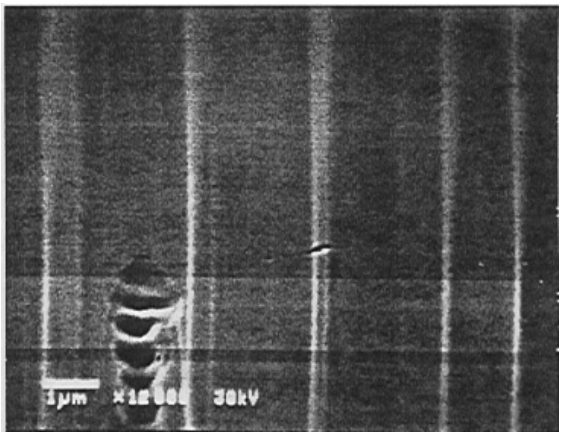

Figure 24 High magnification SEM photo of the HBM failure of the SCR shown in figure 23 for pin 22.

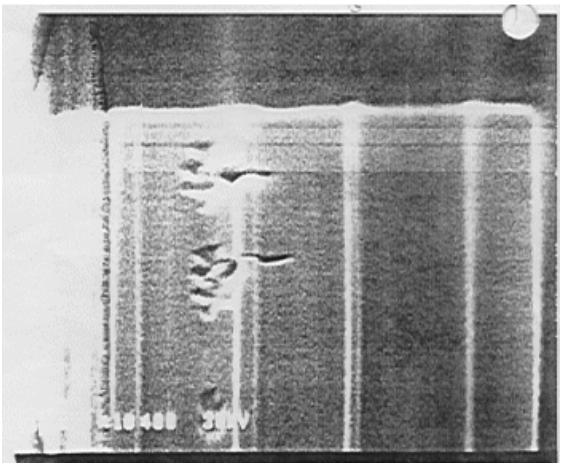

Figure 25 High magnification SEM photo of the HBM failure of the SCR shown in figure 24 for pin 22.

Conclusions

This paper describes an improved measurement technique to demonstrate the ability to correlate electrical failure signatures with the physical failure locations. This improved transmission line pulse (TLP) testing technique was used to show that the electrical failure signature and the physical location for an SCR structure correlated with that of HBM ESD stress testing. The paper demonstrated that the new techniques accurately tracks the leakage current evolution. This leads to better identification of where ESD stress testing should stop and failure analysis begin. Besides the traditional current and voltage measurements at the DUT, this new TLP testing technique included a correction for improved accuracy of the I-V characteristics using a simple short and open for the calibration. The pulse width and rise times of the TLP was chosen to provide the same current amplitude damage level (electrical) as is found in the Human Body Model ESD stress testing. A one to one correlation between the two methods was established which lead to correlation between the electrical damage and the physical location of the failure .

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References

1. L. G. Henry. “Differentiating between EOS and ESD Failures for ICs”. Microelectronic Failure Analysis Desk Reference, 4th Edition, pp421-436. ASM, Materials Park, Ohio, (1999).

2. T. Maloney and N. Khurana, "Transmission Line Pulsing Techniques for Circuit Modeling of ESD Phenomena" EOS/ESD Symposium Proceedings, EOS-7. 1985 pp. 49-54.

3. N. Khurana, T. Maloney and W. Yeh. “ESD on CHMOS Devices – Equivalent Circuits, Physical Models and Failure mechanisms…1985 IEEE IRPS, p212.

4. G. Notermans "On the Use of N Well Resistors for Uniform Triggering of ESD Protection Elements", EOS/ESD Symposium, EOS-19, 1997, p222.

5. S. Kiefer, R. Milburn and K. Rackley: "EOS induced polysilicon migration in VLSI Gate Arrays". EOS/ESD Symposium, EOS-15. 1993, p123-127.

6. W.A. Andersen and D.B. Krakauer. "ESD Protection for Mixed –Voltage I/O Using nMOS Transistors Stacked in a Cascade configuration". EOS/ESD Symposium, EOS-20. 1998, p54-62.

7. G. Notermans, P. de Jong and Fred Kuper. "Pitfalls when correlating TLP, HBM and MM testing". EOS/ESD Symposium, EOS-20, 1998, p170- 176.

8. ESD Association Standard for ESD Sensitivity Testing (Human Body Model). ANSI/EOS/ESD-S5.1-1999.

9. K. Verhaege, P. Roussel, G. Groeseneken, H. E. Maes, H. Gieser, C. Russ, P.Egger, X. Guggenemos and F.G. Kuper. "Analysis of HBM Testers and Specifications Using A 4th Order Lumped Element Model". EOS/ESD Symposium, EOS-15. 1993, p129- 137.

10. S. G. Beebe. Ph.D Thesis, "Characterization, Modeling, and Design of ESD Protection Circuits". 1994. Tech.Report No.ICL94-038, Stanford Univ, Stanford, CA.

11. 11. A. Amerasekera, L. van Roozendaal, J. Abderhalden, J. Bruines, L. Sevat. "An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes". EOS/ESD Symposium. EOS–12. 1990, p143-150.

12. J.C. Smith. "A Substrate Triggered Lateral Bipolar Circuit for High Voltage Tolerant ESD Protection Applications". EOS/ESD Symposium. EOS–20. 1998, p 63-171.

13. H.U. Schroder, G. van Stenwijk and G. Noterman. "High Voltage resistant ESD protection circuitry for 0.5um CMOS OTP/EPROM programming pin". EOS/ESD Symposium. EOS–20. 1998, p 96-103.

14. D. Krakauer and K. Mistry. "ESD Protection in a 3.3V Sub-Micron Silicided CMOS Technology". EOS/ESD Symposium. EOS–14. 1992, p 250-257.

15. N. K. Clark. " Melt Filaments in n+pn+ Lateral Bipolar ESD Protection Devices". EOS/ESD Symposium. EOS–17. 1995, p295-303.

16. J. Z. Chen, A. Amerasekera and C. Duvvury. " Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes." EOS/ESD Symposium. EOS–19. 1997, p230- 239.

17. J. C. Smith. "An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events". EOS/ESD Symposium. EOS–21. 1999, p 62-69.

18. A. Bridgewood and Y. Fu. "A Comparison of Threshold Damage Processses in Thick Field Oxide Protection Devices following Square Pulse and Human Body Model Injection". EOS/ESD Symposium, EOS-10, 1988 page 129.

19. W. Stadler , X. Guggenmos, P. Egger, H. Gieser, C. Musshoff. "Does The ESD-failure Current Obtained by Transmission Line Pulsing always correlate to Human Body Model tests?" EOS/ESD Symposium, EOS-19, 1997. Page 366-372.

20. K. Bock, B. Keppens, V. De Heyn, G. Groesenken, L.Y. Ching and A. Naem. " Influence of Gate Length on ESD-Performance for Deep sub micron CMOS Technology". EOS/ESD Symposium. EOS–21. 1999, p 95-104.

21. H. Gossner, T. Muller-Lynch, K. Esmark and M. Stecher. "Wide Range Control of the Sustaining Voltage of ESD Proptection Elements Realized in a Smart Power Technology". EOS/ESD Symposium, EOS-21, 1999, p19-27.

22. H. Wolf, H. Gieser and W. Wilkening. " Analyzing the Switching Behaviour of ESD- Protection Transistors by Very Fast Transmission Line Pulsing". EOS/ESD Symposium, EOS-21, 1999, p28- 37.

23. K. P. Cheung. "Plasma-Charging Damage and ESD help each other". EOS/ESD Symposium, EOS-21, 1999, p38 – 42.

24. M. Mergens, W. Wilkengang, S. Mettler, H. Wolf, A, Stricker and W. Fichtner. " Analysis and Compact Modeling of Lateral DMOS Power Devices Under ESD Stress Conditions". EOS/ESD Symposium, EOS–21, 1999, page 1-10.

25. C. Russ, K. Bock, M. Rasras, I. DeWolf. G. Groeseneken, H.E. Maes, "Non-Uniform Triggernig of ggNMOSt Investigated by Combined Emision Microscopy and Transmission Line Pulsing", EOS/ESD symposium, EOS-20, 1998, pp177-186.

26. Richier 1997 EOS 19 1997 EMMI only. C. Richier, N. Maene, G. Mabboux and R. Bellens. " Study of ESD behaviour of different clamp configurations in a 0.35 um CMOS technology". EOS/ESD Symposium, EOS-19, 1997, page 240-245.

27. Barth Electronics TLP Application note #3. "TLP to HBM Rise Time Correlation, 1999, Publisher, B.E. Inc, Nevada. www.barthelectronics.com.

28. Leo .G. Henry. Disclosures to the ESDA HBM Working Group (WG–5.2) in 1998 and 1999. "Comparisons between the ESDA and the JEDEC HBM standards".

29. J. Barth, K. Verhaege, Leo G. Henry and John Richner. "TLP Calibrations, Correlation, Standards and New Techniques". Paper accepted by the EOS/ESD Symposium for presentation at the 2000 EOS-22 to be held in Anaheim, CA.

30. H. Ishizuka, K. Okuyama and K, Kubota. "Photo Emission Study of ESD Protection Devices Under Second Breakdown Conditions". The 32nd Annual IRPS, 1994, p286-291.

31. Leo G. Henry, and J.H Mazur. Basic Physics in Color-Coded EOS Metallization Failures-Differentiating between EOS and ESD". The 24th Annual ISTFA, 1998, page 143-150.

32 Leo G. Henry, I. Morgan, M. Merhanpour, T. Raymond. " EOS and ESD Laboratory Simulation and Signature Analysis of a CMOS Programmable Logic Product". The 20th Annual ISTFA, 1994, page117-126 .

33 Barth Electronics TLP Application note #2. "Calibrating TLP Systems", 1999, Publisher, B.E. Inc, Nevada. www.barthelectronics.com.

34. A. Amerasekera and C. Duvvury. ESD in Silicon Integrated Circuits. Publ. John Wiley and Sons, 1995.

35. S. Dabral and T.J. Maloney. Basic ESD and I/O Design. Publ. John Wiley and Sons, 1998.

36. C. Russ, K Verhaege, J. Roussel, G. Groeseneken, and H.E. Maes. "Compact Model for the grounded-gate nMOS transistor behavior under CDM ESD stress", IEEE Transactions on Electron Devices, Vol. 44-11, 1997, pp 1972-1980. And EOS/ESD Symposium, EOS-18, 1996, page 302-315.

37. H. Gieser. "Very-Fast Transmission Line Pulsing of Integrated Structures and the charged Device Model". EOS/ESD Symposium, EOS-18, 1996, page 85-94.